Abstract

A flip-flop circuit with embedded scan capabilities uses a skewed latch to pull one end of the flip-flop either up or down while another end of the flip-flop is active. Further, the flip-flop is designed such that a data node and a scan node are coupled to a master stage, which contains the skewed latch. The data node and scan node values are initially generated from different ends of the flip-flop. Based upon clock dependencies and whether the flip-flop is in a normal mode or a scan mode, the master stage passes a value to a slave stage dependent upon the data node and scan node values. Thereafter, the slave stage outputs a result based on the value passed from the master stage.